REMARKS/ARGUMENTS

In the Final Office Action of January 13, 2010, claims 1 and 3-13 were rejected. However, Applicant hereby requests reconsideration of the application in view of the below-provided remarks.

Claim Rejection under 35 U.S.C. 103

Claims 1, 3, 5 and 9-13 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Stolan (U.S. Pat. No. 5,864,663) in view of Juzswik (U.S. Pat. No. 4,698,478). Claims 4 and 6-8 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Stolan in view of Juzswik and further in view of Ubicom (Ubicom Product Report –IP2022 Internet Processor, hereinafter "Ubicom"). However, Applicant respectfully submits that the pending claims are patentable over Stolan, Juzswik and Ubicom for the reasons provided below.

Independent Claim 1

Claim 1 recites:

"A method of monitoring the operation of a microcontroller unit that is intended for at least one application and is associated with a system, by means of a base chip, particularly a system base chip, characterized in that:

causing a reset of the microcontroller unit if a reset condition is detected, wherein the reset condition is transmission of at least one special sequence, particularly at least one drive or access sequence assigned to the reset operation, to the base chip and the reset of the microcontroller unit is confirmed under an enquiry routine by checking whether the at least one special sequence has been successfully transmitted to the base chip;

activating a special mode of operation, particularly a flash mode of the base chip, once after the check has been made to see whether the special sequence has been successfully applied and after the reset operation, by allowing access to a monitoring module that is associated with the base chip to take place in a manner which is simplified in comparison with the normal mode of operation of the microcontroller unit;

supplying a permanent energy supply from a battery unit to the monitoring module; and

switching a microcontroller supply unit of the base chip to enable or disable a temporary energy supply from the battery unit to the microcontroller unit."

Applicant respectfully submits that a *prima facie* case of obviousness has not been established with respect to claim 1. Applicant respectfully asserts that claim 1 is not obvious over Stolan in view of Juzswik because the proposed combination of Stolan and Juzswik would change the function of the microprocessor (12) of Stolan.

MPEP §2143.02 states:

> "A rationale to support a conclusion that a claim would have been obvious is that all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with **no change in their respective functions**, and the combination would have yielded nothing more than predictable results to one of ordinary skill in the art. *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, ___, 82 USPQ2d 1385, 1395 (2007); *Sakraida v. AG Pro, Inc.*, 425 U.S. 273, 282, 189 USPQ 449, 453 (1976); *Anderson's-Black Rock, Inc. v. Pavement Salvage Co.*, 396 U.S. 57, 62-63, 163 USPQ 673, 675 (1969); *Great Atlantic & P. Tea Co. v. Supermarket Equipment Corp.*, 340 U.S. 147, 152, 87 USPQ 303, 306 (1950)." (emphasis added)

The Office Action on page 3 recognizes that "Stolan does not explicitly disclose the steps of supplying a permanent energy supply from a battery unit to the monitoring module; and switching a microcontroller supply unit of the base chip to enable or disable a temporary energy supply from the battery unit to the microcontroller unit." However, the Office Action then alleges that "Juzswik discloses using this technique [col. 2, line 32 – col. 3, line 4] for the purpose of reducing power consumption in a system having a microprocessor and a watchdog timer."

Stolan discloses a system that includes the microprocessor (12) and a watchdog timer circuit (10). (See Figs. 1 and 2, and column 4, lines 43-65 of Stolan). Stolan further discloses that the watchdog timer circuit (10) includes a counter (18) and that the microprocessor (12) is programmed to check a most significant bit (MSB) status of the counter (18) every millisecond. (See column 4, line 58 of Stolan). Additionally, Stolan discloses that if the MSB is found not to be logic high, the microprocessor (12) sends a count up signal to the counter (18) and exits the counter checking program and that if the MSB is found to be logic high, the microprocessor (12) sends a count down signal to the counter (18) and exits the counter checking program. (See Fig. 3 and column 5, lines 31-45 of Stolan). That is, Stolan teaches that the function of the microprocessor (12) involves checking the watchdog timer circuit (10) every millisecond.

Juzswik teaches a system for controlling body electrical requirements of an automotive vehicle and monitoring various essential switch conditions to ascertain the level of activity. (See column 2, lines 31-35 of Juzswik). Juzswik further teaches that after the system enters the "sleep" mode, the system will wake up briefly some 600 or 700 milliseconds later and repower the control system sufficiently to again check the essential inputs and return to another sleep mode if no activity has occurred to conserve power. (See column 1, lines 9-11 and column 3, lines 13-18 of Juzswik). That is, Juzswik teaches that the function of the system for monitoring the essential switch conditions involves sleeping and then waking up after 600 or 700 milliseconds to conserve power.

Thus, if the microprocessor (12) of Stolan is combined with the system for monitoring the essential switch conditions of Juzswik, the microprocessor (12) of Stolan would be changed to check the MSB status of the counter (18) in the watchdog timer circuit (10) after 600 or 700 milliseconds of sleep. As a result, the proposed combination of Stolan and Juzswik would prevent the microprocessor (12) of Stolan from checking the MSB status of the counter (18) in the watchdog timer circuit (10) every millisecond. Therefore, Applicant respectfully submits that the proposed combination of Stolan and Juzswik would change the function of the microprocessor (12) of Stolan. Because the proposed combination of Stolan and Juzswik would not result in elements with **no change in their respective functions**, Applicant respectfully submits that claim 1 is not obvious over Stolan in view of Juzswik.

Dependent Claims 3, 4, 10 and 11

Claims 3, 4, 10 and 11 depend from and incorporate all of the limitations of independent claim 1. Thus, Applicant respectfully asserts that claims 3, 4, 10 and 11 are allowable at least based on an allowable claim 1.

Independent Claim 5

Claim 5 includes similar limitations to claim 1. Because of the similarities between claim 5 and claim 1, Applicant respectfully asserts that the above remarks with regard to claim 1 apply also to claim 5. Accordingly, Applicant respectfully submits that

the teachings of Stolan in view of Juzswik are not sufficient to render claim 5 *prima facie* obvious.

Dependent Claims 6-9, 12 and 13

Claims 6-9, 12 and 13 depend from and incorporate all of the limitations of independent claim 5. Thus, Applicant respectfully asserts that claims 6-9, 12 and 13 are allowable at least based on an allowable claim 5.

Double Patenting Rejection

Applicant notes herein that the alleged double patenting rejections will be addressed at a later time, assuming that these rejections are still applicable.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted on behalf of:

NXP N.V.

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By: /thomas h. ham/
Thomas H. Ham
Reg. No. 43,654

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111